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Low-Power and Space-Efficient Built In Self-Test Architecture With MSIC Test Pattern Generator

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ABSTRACT

The new low-cost test pattern generation approach for a Multiple Single Input Change (MSIC) test pattern BIST architecture. BIST is a methodology that uses on-chip test logic to identify problematic system components. To increase fault coverage, the authors propose using a test pattern generator that creates MSIC test patterns and weights the pseudorandom test patterns. The goal is to provide an effective weighted TPG for a BIST architecture based on scans that requires less space and power usage. To maximize the length of the weighted pseudorandom patterns, the authors use a TPG pseudo-primary seed and a weight-enabled clock to provide distinct weights to the various scan chains. By this method, the hardware overhead is decreased and 0.215 µW power usage is achieved . The proposed weighted TPG produces accurate results when applied to two alternative test-per-scan BIST architectures, with fewer switching transitions, larger fault coverages, and less delay of 0.170 µs and area compared to existing methods. This behavior is observed for six additional circuits being tested. In order to compare the suggested balanced TPG with other potential designs, it is also scaled up to a larger bit TPG. The experimental findings are compared and contrasted with those of other TPG designs.

Keywords: *BuiltInSelfTest(BIST), Multiple single input change(MSIC), Test pattern generator(TPG), fault coverage, pseudorandom test pattern*

INTRODUCTION

Built In Self Test, is a structural testing ,that the involves adding logic to an integrated circuit (IC) so that the IC can periodically evaluate its own performance. The two primary forms of BIST are memory and logic. Memory BIST, also referred to as MBIST, develops memory specific patterns and scans them to detect any defects.

Redundancy and repair features are also included in Memory BIST. In this method, a backup circuit is included into each die. A good circuit is plugged in when a circuit is broken, and the damaged one is unplugged. is put in position in its place. Memory BIST is also used for 2.5D/3D devices to get well-known good memory stacks.

With the use of a pseudo-random number generator, logic BIST, also known as LBIST, creates input patterns that are then applied to internal scan chains. With the use of a pseudo-random number generator, logic BIST, also known as LBIST, creates input patterns that are then applied to internal scan chains. pattern generator. The results are compressed to form a signature. A Multi-Input Signature Register then assesses the accuracy of the signature to determine whether or not all tests were successful. The most widespread use of LBIST is in automotive and other high-reliability, safety-critical applications. Yet, LBIST requires a very clear design because unidentified states would hinder functionality.

As a result, design and test criteria must be tougher, and LBIST insertion is more challenging than scan. LBIST also experiences significant timing, space, and power overhead. Built-in self-test, sometimes known as BIST, is a DFT technique that entails adding extra hardware and software capabilities to integrated circuits so they may conduct their own testing, hence reducing utilising an external ATE and cutting testing expenditures. Almost all sorts of circuits may use the BIST approach. BIST is a method for testing circuits. It including embedded memory utilised by internal devices, that do not have direct connections to external pins.. In BIST, test patterns are created by a test pattern generator, and test responses are compared by a signature analyzer (SA). The BIST controller oversees the entire procedure. LBIST, which is intended in order to test random logic, devices are often equipped with multiple input signature registers (MISRs) that record how the device responds to test input patterns and pseudorandom pattern generators that produce input patterns that are applied to the device's internal scan chain. An erroneous MISR output is indicative of a device fault. In order to assess memory, MBIST was created. A series of write-read-write memory sequences are typically seen in test circuits. MarchC, Walking 1/0, GalPat, and Butterfly are examples of sophisticated write-read sequences, or algorithms.. It looks into the financial effects of logic and memory cores that have built-in self-testing. Implementing BIST has several advantages, including better testability and fault coverage support for concurrent testing, lower test costs owing to the elimination or reduction of the need for external electrical testing using an ATE, and quicker test timeframes. Whether the BIST can be constructed to swiftly and concurrently test a number of structures.Using mathematics found in queuing theory, these and other parameters can be added to a maintainability model. By modifying values and utilising maintainability margins in various ways, this enables manipulating maintainability metrics in "what-if" analysis, which can be useful in resolving maintainability difficulties. In order to ensure that the allocations are in line with top-level figures, the model may also be set up to compute an aggregate maintainability figure from the several lower-tier data.

The mean time between maintenance (MTBM) and mean time between failures (MTBF) reliability characteristics are equivalent when neither preventative maintenance nor failures resulting from maintenance are present.The maintainability engineer should create and maintain a model of the requirements for maintainability that is also capable of producing a report whose content is based on the information needs of the client.you can frequently expect to submit extensive data on corrective maintenance, a mean time to repair (MTTR) summary, and data on turnaround or preventive maintenance.They are many methods to evaluate maintainability and numerous ways to monitor time spent doing maintenance activities, therefore this client must very carefully specify and authorise the corrective repair times. These timings may simply apply to time-of-line replaceable units that can be removed and replaced or they may also apply to access, checkout, and logistical delays. Every component that has been approved for the durability programme should have its assigned corrective repair times tabulated by the maintainability engineer (preferably in a computer database model). Assigned repair hours are multiplied by assigned failure rate figures for each component included in the maintenance analysis, taken from the reliability analysis. A measure of MTTR is produced by adding these products and dividing the result by the total number of allotted failure rates. The MTTR in this instance would be

J Popul Ther Clin Pharmacol Vol 30(9):e308–e314; 05 April 2023.

0.3500,when something breaks, it takes 21 minutes (0.35 x 60).It is calculated using a weighted average of the component figures.

RELATED WORK

A innovative approach for developing faultaware memory BIST infrastructure is presented by G. Harutyunyan [2018] and is based on test algorithms and principles in recollections, of fault periodicity and regularity. The Test Algorithm Template (TAT) and the Fault Periodicity Table (FPT) are two separate internal structures that specify these periodicity and regularity concepts. Cells, multilayered storage circuits, and other memory-storing components are all part of systems for Systems-on-Chip and scattered over various sub chips, are taken into consideration as the three dimensions of evolution that go into the formation of the aforementioned structures. Each row of the FPT refers to a fault family, which is distinguished by the intensity of fault sensitization, and every column of the FPT refers to a type of fault that may be associated with a number of various test techniques.When TAT enables the creation of test algorithms without the use of test algorithm generation tools, FPT permits the consideration of any big number of defects in one table. The system was tested using FinFETbased (16/10/7nm) and Planar-based (90/65/45/28nm) memory technology,with similar results. Resources are a crucial consideration when deciding how to proceed because, in some cases, it may be impractical to keep generating new models. Instead, it may be more costeffective to reframe an existing, versatile model.

FAST was given a fully autonomous built-in self-testing strategy by Matthias Kampmann [2019] in this publication. This method makes infield testing easier by employing the proper test creation and response compaction techniques. To cut down on test time and hardware overhead, the necessary Certain frequency test for detection are established. Test response compaction, which saves interim MISR signatures in a little on-chip memory for X canceling transformation analysis later, further addresses the vast quantity of unknown values along lengthy pathways.The potency of the suggested strategy is demonstrated by a thorough experimental research.The effect of the considered fault size is specifically and thoroughly explored.

The next-generation automotive architecture has been built using an automobile flash MCU with a 28nm, 600-MHz, according to a report presented by Hiroyuki Kondo [2020]. Three essential features are integrated into the MCU for vehicle control: an in-vehicle network serial gigabit media independent interface (SGMII),a built in self test in the field, and a virtualizationassisted processor (VAP) for functional safety. The VAP enables real-time virtualization by assisting the hypervisor. so that numerous virtual machines can run independently of one another. In numerous automotive applications, the SR BIST realises error per hour of 108. Because 5-V transistors have excellent dependability while having a small bandwidth, we used them in the SGMII circuit. The MCUs in automobiles 0.52 W low power consumption satisfies the ISO 26262 ASIL D system criteria. The severe automotive control hard real time capacity is realisable by the VAP.

A method was put up by Vishnupriya Shivakumar [2021] that lowers hardware overhead while achieving a 26.7 nW low power consumption. However, the proposed weighted TPG produces accurate results when applied to two alternative test-perscan BIST architectures. Fewer switching transitions and greater fault coverages of 98.81% and 97.35% are also achieved in the weighted patterns of two separate BIST designs. This behaviour is noted as the scan chains for the additional six circuits are tested. The results of the simulation are verified with the Mentor Graphic IC design platform's SilTerra 0.13 m process. To carry out the performance plans, the Moreover, the bit TPG for proposed weighted TPG is raised and compared. This proposed TPG design's experimental findings are summarized and compared to those of other prospective TPG designs.

A model predictive control (MPC) technique was presented for multi-port modular multilevel converters by Mohamed Badawy [2021] MPMMCs.The usage of hybrid energy storage devices is simplified by the use of MP-MMCs in a scalable energy management system (EMS) for

EV applications (HESDs). Using this method, the number of high-power inverters and their filtering is decreased. parts and size and weight of the EV drivetrain. Future electrified transportation systems will require an EMS to control the energy flow from the cells and keep their charging/discharging rates within the desired operating ranges.

EXISTING METHOD

An entirely distinct lower-power balanced TPG is suggested for the present technique in order to produce effective balanced patterns. Mathematically, the operation of Galois is used to determine the first pseudo-primary seed bits' subset, resulting in the longest possible weight patterns with the fewest transitions. The test's per check approach uses the balanced Mux, which limits switching transitions by acting a shifter of phases in the design. A 32-bit TPG is enhanced to be implemented with the suggested weighted TPG, making sure there is little space overhead and low power usage during the clock cycle. The PDP for the recommended design accomplishes this as a result a reduction of about 43.3% when compared to the current TPGs. According to experimental findings, the suggested TPG's performance criteria are superior than those of other TPGs. To demonstrate WSA reductions and enhanced fault coverage, this work is applied to two different BIST architecture included, the WSA savings were 25.5%; when considered, they were 23.5%. For transition delay faults, the fault coverage is largely complete. This work may be be expanded to realise sequential, redundant, screening and capturing a changes in phase, stuck-open and other faults. The various BIST scan-forest topologies can also use this strategy.

PROPOSED SOLUTION

In this proposed system, a new MSIC TPG for a checks determined structure. The proposed TPG is designed using low-cost test pattern generation schemes for a Multiple single input change (MSIC) test pattern BIST architecture. This system architecture of SIE module is illustrated. Data input is obtained at the transmitter end. For the incoming data, it is recommended to do packet format analysis and categorization beforehand. The input data are transmitted to the receiving end upon the completion of the aforementioned processing. The onus of ensuring that the data received are correct rests with the receiving end. In the suggested TPG design's operation of Galois, the fixed pseudo primary seeds are expanded. The main advantages of the proposed system are:

Fewer switching transitions.

The TPG enhances its quick switching activity.

Lowers the average amount of electricity used for scanning and capturing.

Improves the fault coverage.

METHODOLOGY

Weight Enable Clock

Fewer switching transitions are obtained utilising the particular weighted patterns, and lower power is achieved by using fewer hardware components in the suggested weighted TPG's architecture. As a result, the hardware overhead is decreased and the BIST's fault coverage is enhanced. The planned TPG depicts the Galois operation as a dark dotted line. This process is simplified by assuming that the pseudo primary seeds (A, X) are fixed. The fixed seed bits' can be expanded using the similar set of starting primary seeds. The longest possible duration in scaled patterns with reduced shifting operation may be determined using these seed subgroups.

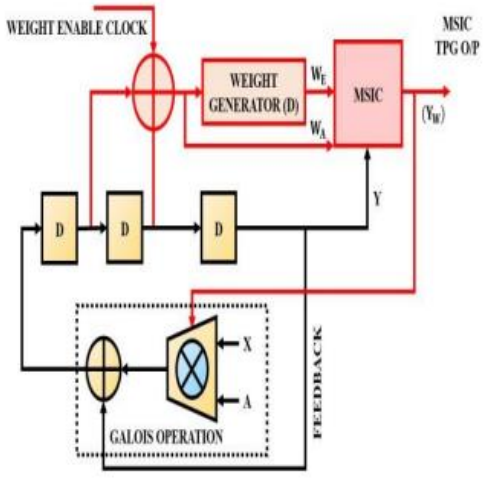

FIG.4.1 Proposed -MISC TPG

J Popul Ther Clin Pharmacol Vol 30(9):e308–e314; 05 April 2023.

Weight Generator

In the BIST architecture, the fault coverage for redundant and random-pattern resistant faults is effectively decreased by the weight generator clock choice. The Galois technique is used to propose a 3-bit pseudorandom TPG over a GF field. (2m). Shift registers and the Galois operation are used simultaneously to construct the test patterns. The TPG's synchronous clock results in the loss of bit sequences when utilized for m-bits. The weightenabled clock and weight generator appear to be part of a system that controls or regulates a process using probability-based methods. Yet, it is impossible to offer a more particular interpretation or application of this technology without further context or knowledge.

MSIC

The MSIC test pattern generator creates test patterns with changes to only one bit position, or a minimum transition sequence. The shifting operation of the test circuit, the scan chains, and eventually their use of electricity are lowered by increasing the relation among the designs as well as inside every design in the generated scan loop. Shifting operation that causes mistake is decreased even though test pattern repetition is a possibility in the MSIC sequence produced by the MSIC test pattern generator. So the system improves the test efficiency. Moreover, this technique lowers the amount of time needed to move between test patterns when in testing mode.

MSIC TPG Output

Using Xilinx 13.2, MSIC TPG performance simulations and CUT testing are performed. The suggested MSIC test pattern generator's simulated output. One can conclude that the test pattern creation if the MSIC TPG-created test patterns offer the desired output of the circuit being tested without any errors.

Galois Operation

For simplicity, the dark dotted line indicates the operation of Galois in the suggested TPG, which is based on the assumption of fixed pseudo primary seeds (A ,X).Yet, the same subset of the initial primary seeds can be used to expand the constant seed bits . When switching activity is lower in weighted patterns, the maximum length is obtained using the seed subsets. The blue line represents more technology that uses fewer components to generate the balanced pseudorandom TPG result. In compared to other TPG approaches. The suggested TPG achieves its weighted pattern with fewer components, including adder and multiplier in the operation of Galois .

Feedback

The outgoing feedback signal and the incoming seed bits are used to implement the TPG linear function. Its linear properties are used in a range of functions including as power distribution and production systems, audio and video systems, medical systems, cockpit systems, and aviation systems. The registers' current state allows for similarity on multiple levels. The feedback loop structure is used to describe the (j+1)-th level following the j^th level.

TABLE 1: compares the bitwise performances of the proposed and current systems.

	Power Consumption (μW)	Delay (μs)	Area	Software Used
Existing System	0.318 μW	0.531 μs	9214.2	Xilinx ISE 12.4
Proposed System	0.215 μW	0.170 μs	4263	Xilinx ISE 13.4

RESULTS

As shown in Figure 5.1, the data transmission module can be synchronized at far greater frequencies than typical conservative design (up to 1.5 times higher frequency), because the circuit was designed using the BIST assertive layout method for any any given NoC

components (such as switches,links,and network interfaces)

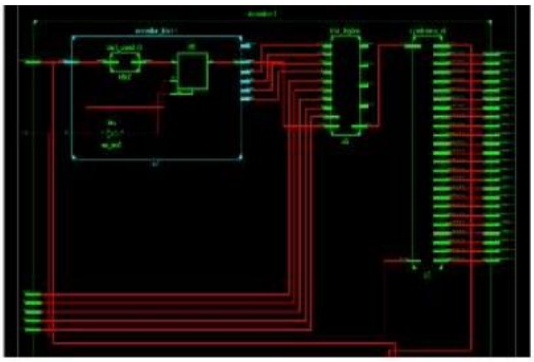

FIG.5.1: Schematic Diagram

Figure 5.2 illustrates that the circuit for borrowing time from the next path of following logic requires a longer route. As time borrowing slows down data arrival time and increases data arrival time, it often has an impact on setup. It has no impact on the wait time since the hold period has a longer data arrival time.

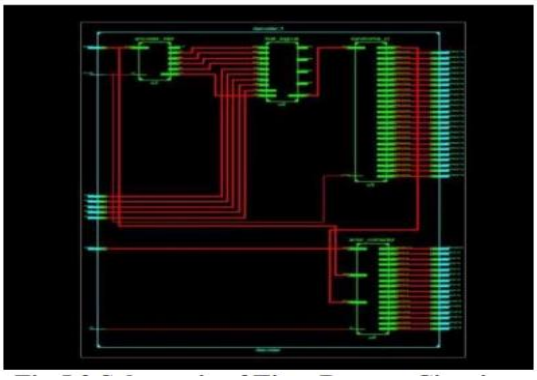

FIG 5.2 Schematic of Time Borrow Circuit

FIG.5.3 Simulated Output Before the Error Correction

FIG.5.4 Simulation Output After the Error Corrected

Figure 5.4 perfectly demonstrates the simulation's outcomes when the error is corrected, that is it will shows that there is no error and display that result as corrected.

CONCLUSION

In this project, a fresh MSIC TPG for a scan-based architecture is proposed. The power consumption and area are reduced, by using an efficient MSIC test pattern stands for multiple single input change. The occurrence of error is prevented during the transmission of data from one place to another. Only fewer switching transitions are achieved using the specific MSIC test pattern. A class of SIC sequences known as MSIC was recovered from a theory that expresses a sequence produced by linear sequential structures. According to the analysis's findings, The benefits of an MSIC sequence's uniform distribution, a trivial input and a trivial relation among the test duration and the TPG's early stages. The MSIC-TPG may be used method-per-clock and method-per-scan tests and it is simple to construct.

REFERENCES

1. G. Harutyunyan, S. Shoukourian and Y. Zorian, "Fault Awareness for Memory BIST Architecture Shaped by Multidimensional Prediction Mechanism," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 3, pp. 562-575, March 2019, doi: 10.1109/TCAD.2018.2818688.

J Popul Ther Clin Pharmacol Vol 30(9):e308–e314; 05 April 2023.

2. M. Kampmann, M. A. Kochte, C. Liu, E. Schneider, S. Hellebrand and H. -J. Wunderlich, "Built-In Test for Hidden Delay Faults," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 10, pp. 1956-1968, Oct. 2019, doi: 10.1109/TCAD.2018.2864255.
3. H. Kondo et al., "A 28-nm Automotive Flash Microcontroller With Virtualization-Assisted Processor Supporting ISO26262 ASIL D," in IEEE Journal of Solid-State Circuits, vol. 55, no. 1, pp. 133-144, Jan. 2020, doi: 10.1109/JSSC.2019.2953826.
4. V. Shivakumar, C. Senthilpari and Z. Yusoff, "A Low-Power and Area-Efficient Design of a Weighted Pseudorandom Test-Pattern Generator for a Test-Per-Scan Built-in Self-Test Architecture," in IEEE Access, vol. 9, pp. 29366-29379, 2021, doi: 10.1109/ACCESS.2021.3059171.
5. G. N. Balaji and S. C. Pandian, ‘‘Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates,’’ Cluster Comput., vol. 22, no. S6, pp. 15231–15244, Nov. 2019, doi: 10.1007/s10586-018-2552-x.
6. X. Lin and J. Rajski, ‘‘Adaptive low shift power test pattern generator for logic BIST,’’ in Proc. Asian Test Symp., 2010, pp. 355–360, doi: 10.1109/ATS.2010.67.
7. S. Hellebrand, S. Tarnick, J. Rajski, B. Courtois, and T. I. M. Imag, ‘‘Multiple-polynomial linear feedback shift registers,’’ 1992, pp. 120–129
8. G. S. Sankari and M. Maheswari, ‘‘Energy efficientweighted test pattern generator based bist architecture,’’ in Proc. Int. Conf. I-SMAC (IoT Soc. Mobile, Anal. Cloud), I-SMAC, 2019, pp. 448–453, doi: 10.1109/ I-SMAC.2018.8653768.
9. A. S. Abu-Issa, ‘‘Energy-efficient scheme for multiple scan-chains BIST using weight-based segmentation,’’ IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 3, pp. 361–365, Mar. 2018, doi: 10.1109/TCSII.2016. 2617160.
10. A. Jas, C. V. Krishna, and N. A. Touba, ‘‘Weighted pseudorandom hybrid BIST,’’ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 12, pp. 1277–1283, Dec. 2004, doi: 10.1109/TVLSI.2004.837985.
11. R. Kapur, S. Patil, T. J. Snethen, and T. W. Williams, ‘‘A weighted random pattern test generation system,’’ IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 15, no. 8, pp. 1020–1025, Aug. 1996, doi: 10.1109/43.511581.
12. H.-C. Tsai, K.-T. Cheng, and S. Bhawmik, ‘‘On improving test quality of scan-based BIST,’’ IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 19, no. 8, pp. 928–938, Aug. 2000, doi: 10.1109/ 43.856978
13. D. Xiang, M. Chen, and H. Fujiwara, ‘‘Using weighted scan enable signals to improve test effectiveness of scan-based BIST,’’ IEEE Trans. Comput., vol. 56, no. 12, pp. 1619–1628, Dec. 2007.
14. G. Kiefer, H. Vranken, E. J. Marinissen, and H. J. Wunderlich, ‘‘Application of deterministic logic BIST on industrial circuits,’’ J. Electron. Test. Theory Appl., vol. 17, nos. 3–4, pp. 351–362, 2001, doi: 10.1023/A:1012283800306.
15. N. A. Touba and E. J. McCluskey, ‘‘Altering a pseudo-random bit sequence for scan-based BIST,’’ in Proc. IEEE Int. Test Conf., Oct. 1996, pp. 167–175, doi: 10.1109/test.1996.556959.
16. B. W. Johnson, J. H. Aylor, and H. H. Hana, ‘‘Efficient use of time and hardware redundancy for concurrent error detection in a 32-bit VLSI adder,’’ Comput. Arith., vol. 23, no. 1, pp. 171–178, 2015, doi: 10.1142/9789814641470